Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	9	((pile adj up) with density with dislocation) and germanium	US-PGPUB; USPAT	OR	ON	2005/02/23 15:16
L2	9	1 and 2ad<"22020823"	US-PGPUB; USPAT	OR	ON	2005/02/23 15:11
L3	1	((pile adj up) with density with dislocation) and germanium	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/02/23 15:16

US-PAT-NO: 6039803

DOCUMENT-IDENTIFIER: US 6039803 A

TITLE: Utilization of miscut substrates to improve relaxed graded silicon-germanium and germanium layers on silicon

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Brief Summary Text - BSTX (4):

Growing relaxed graded layers of Si--Ge substrates at approximately 800.degree. C. is known to produce quality layers with low defect densities. Grading up to 100% Ge on conventional on-axis Si(001) substrates, however, results in large surface roughness and a high **density** of defects such as **dislocation pile-ups**.

Brief Summary Text - BSTX (9):

In accordance with the invention, (001) silicon substrates that are off-cut towards a <110> direction by 6.degree. are used in the growth of graded Si--Ge layers. In the layers graded up to 100% Ge, there is a substantial improvement in the surface roughness and **dislocation pile-up densities** as compared to growth on the conventional Si(001) on-axis substrates. The present invention involves the use of miscut Si(001) substrates and obtained improved layer quality in terms of surface roughness and **dislocation pile-up densities**. The root mean square (rms) surface roughness measured using atomic force microscopy (AFM) shows a 75% improvement for samples graded up to 100% Ge over growth on the conventional on-axis Si(001) substrates. The **dislocation pile-up densities** measured using electron beam induced current (EBIC) were about an order of magnitude lower for the 100% Ge samples grown on the off-cut Si substrates as compared to growth on the on-axis Si substrates. Thus, the use of off-cut Si substrates results in a tremendous improvement in the quality of graded Ge layers grown on Si.

Brief Summary Text - BSTX (10):

The reduced surface roughness translates into ease of subsequent processing for GaAs growth. A lower surface roughness also helps in easy patterning of the Ge surface for device processing. Reduced **dislocation pile-up density** implies that the material has improved electronic properties.

Drawing Description Text - DRTX (10):

FIG. 8 is a bar graph showing the correlation between the observed rms roughness and **dislocation pile-up density** along the two in-plane <110> directions for Ge/Ge.sub.x Si.sub.1-x /Si samples graded up to 100% Ge grown on the on-axis exact (001) and 6.degree. off-cut (001) Si substrates;

Detailed Description Text - DETX (2):

The present invention is directed to the use and effect of substrate miscut on the surface morphology and the dislocation structure in Ge/Si--Ge(graded)/Si. It will be appreciated by those of skill in the art that a criterion exists for the arrest of a threading dislocation in a strained epitaxial layer due to interaction with the stress field of an orthogonal misfit dislocation lying in its path, as described in L. B. Freund, J. Appl. Phys. 68, 2073 (1990), incorporated herein by reference. By applying the dislocation blocking criterion to graded Si--Ge structures with a rough surface, it is possible to predict the formation of dislocation pile-ups from the maximum trench depth of the cross hatch pattern. The **pile-ups** are not only deleterious because they contain a high threading **dislocation density,** but they lead to extremely rough surfaces due to stress-related growth instability.

Detailed Description Text - DETX (5):

It will be appreciated that with respect to the present invention, even gradual roughness such as those present in slowly graded samples, leads to the formation of dislocation pile-ups in graded buffers under prolonged relaxation. The **pile-ups** increase the threading **dislocation density** in the relaxed Ge-Si/Si structures. By growth on off-cut wafers, the surface roughness decreases drastically and the pile-up density decreases as well. It is proposed that threading dislocations are not easily blocked by non-parallel misfit dislocations. In addition, it is possible to form an alternative dislocation array to the 60.degree. dislocation array normally present in graded relaxed mismatched heterostructures. With respect to the present invention, in Ge rich regions of the graded Ge.sub.x Si.sub.1-x structures, a large number of edge dislocations of the type 1/2<110 > as well as in-plane Burgers vectors of the type <100> have been observed. Four 1/2<110> edge dislocations and two <100> edge dislocations lead to a lower energy hexagonal dislocation network. Such a dislocation network, first reported in bulk silver bromide crystals, has not been previously characterized in lattice mismatched heteroepitaxial thin films. The present invention suggests that favorable intersection of the [111] glide planes in exemplary samples grown on the miscut substrates aid the dislocation reactions necessary to form this network.

Detailed Description Text - DETX (11):

Electron beam inducted current (EBIC) was used to observe electrically

active dislocations threading up through the uniform cap layer. The threading segments of dislocations gliding on the [111] planes can interact with stress fields of pre-existing orthogonal misfit dislocations and get trapped. Other factors like surface trenches can aid such blocking. This blocking can create dislocation pile-ups along trenches in the cross hatch pattern. These pile-ups were good recombination sites for charge carriers and showed a dark contrast along the trenches. The **dislocation pile-ups** are planar defects and their **densities** were characterized by the number of intersections per unit length of the sample surface. The density (no./cm) was determined by calculating the number of intersections of the dark contrast lines with random straight lines drawn on the EBIC micrographs.

Detailed Description Text - DETX (12):

The following is a summary of the experimental data collected from the Ge/Ge.sub.x Si.sub.1-x /Si films grown on off-cut and on-axis (001) Si wafers. FIG. 1B is a plot showing increase in threading dislocation density with increasing final Ge % in the graded layer. FIG. 1 shows the trend in threading dislocation density versus final Ge concentration in graded 10% Ge/.mu.m layers. If it is desired to integrate devices on these buffers, the origin of this dislocation increase must be determined. The threading **dislocation density** increase can be correlated to **pile-up density** and surface roughness. For this constant grading rate, one does not expect an increase in threading dislocation density unless there is a decrease in average misfit dislocation length. Thus, one possibility is that dislocation interactions that arrest dislocation motion must become more probable with thicker graded layers. In addition, the increase in threading **dislocation density** can be correlated to surface roughness and **dislocation pile-up density**. In the following description, initially the observations of surface morphology and pile-up density on on-axis wafers will be discussed, followed by the effect of off-cut wafers on defect morphology.

Detailed Description Text - DETX (29):

A correlation between rms roughness and **dislocation pile-up density** for Ge/Ge.sub.x Si.sub.1-x /Si(001) samples, as shown in FIG. 8, along the two in-plane <110> directions agrees with the above analysis. FIG. 8 shows a graph of the correlation between the observed rms roughness and **dislocation pile-up density** along the two in-plane <110> directions for Ge/Ge.sub.x Si.sub.1-x /Si samples graded up to 100% Ge grown on the on-axis exact (001) and 6.degree. off-cut (001) Si substrates. It was found that a high rms roughness was associated with a high **dislocation pile-up density** for a given direction on the sample surface.

Detailed Description Text - DETX (34):

FIGS. 9A and 9B are plan view EBIC images of Ge/Ge.sub.x Si.sub.1-x /Si samples graded up to 100% Ge grown on Si(001) exact and Si(001) 6.degree. off-cut towards <110> Si substrates, respectively. The images illustrate the drastic reduction in **dislocation pile-up density** for the sample grown on the off-cut substrate. For the sample grown on the off-cut substrate, there is a clear anisotropy in the density of pile-ups along the two in-plane <110> directions.

Detailed Description Text - DETX (35):

The plot of FIG. 6 predicts that the samples graded up to 70% Ge and 100% Ge would form dislocation pile-ups. It was found to be true for the 100% Ge samples grown on Si(001) and Si(001) off-cut substrates, as shown in FIGS. 9A and 9B. There is a substantial reduction in **dislocation pile-up density** in the 100% Ge sample grown on an off-cut substrate. As previously described, growth on an (001) off-cut substrate results in reduced surface roughness and reduced trench depths. In FIG. 6, the "maximum trench depth" point for the off-cut sample is close to the h* line indicating that there are only a few deep trenches that can cause dislocation blocking. Hence, it is not surprising that the **dislocation pile-up density** is extremely low for growth on the off-cut substrate. As shown in FIG. 8, there was a clear anisotropy in the **dislocation pile-up density** along the two in-plane <110> directions in case of the 100% Ge sample grown on an off-cut substrate. The anisotropy in **dislocation pile-up density** is related to the anisotropy or rms roughness previously described. Anisotrophy in surface roughness and **dislocation pile-up density** of a much lesser degree is also observed in the 100% Ge (001) exact oriented sample. This anisotrophy is probably related to unintentional miscut in the substrate.

Detailed Description Text - DETX (45):

Accordingly, the origin of dislocation pile-up formation and surface roughness in graded Ge/Ge.sub.x Si.sub.1-x /Si layers has been investigated. The effect of substrate off-cut on surface morphology, dislocation pile-up formation and the dislocation structure was studied as well. Dislocation pile-ups originate from a combination of dislocation interaction and the effect of surface morphology. The exemplary samples grown on (001) off-cut substrates showed reduced surface roughness and a low **dislocation pile-up density** as compared to samples grown on (001) exact oriented substrates. A model was proposed to explain the formation of dislocation pile-ups in graded structures. Applying both dislocation blocking criterion and the impact of surface morphology to gliding dislocations, and studying the effect of maximum trench depth of the cross hatch pattern, it was possible to predict the likelihood of

dislocation pile-up formation. Off-cut wafers decrease the chance of **dislocation pile-up** formation, leading to lower **pile-up densities** and smoother surfaces. Additionally, reduced roughness is expected due growth rate anisotrophy and the ease of formation of edge dislocation (that are less effective in inducing inhomogeneous strain fields at the surface).

Claims Text - CLTX (3):
epitaxially growing a relaxed graded layer of a crystalline second semiconductor material on said substrate, said second semiconductor material including at least said first semiconductor material, and thus forming a semiconductor surface of the relaxed graded layer that has a **dislocation pile-up density** less than 60 per centimeter, and a threading **dislocation density** lower than 3.times.10.sup.6 cm.sup.-2 and a root-mean square surface roughness of less than 20 nm.

Claims Text - CLTX (16):
epitaxially growing a relaxed graded layer of crystalline second semiconductor material on said substrate, said second semiconductor material including at least said first semiconductor material, and thus forming a semiconductor surface of the relaxed graded layer that has a lower **dislocation pile-up density** less than 60 per centimeter, and a threading **dislocation density** lower than 3.times.10.sup.6 cm.sup.-2 and a root-mean-square surface roughness of less than 20 nm.

Claims Text - CLTX (19):
a relaxed graded layer of a crystalline GeSi which is epitaxially grown on said substrate, wherein a semiconductor surface of the relaxed graded layer has a **dislocation pile-up density** less than 60 per centimeter, and a threading **dislocation density** lower than 3.times.10.sup.6 cm.sup.-2 and a root-mean-square surface roughness of less than 20 nm.